LATERAL SEMICONDUCTOR ARRANGEMENT FOR POWER ICS

This is a continuation-in-part of application Ser. No. 08/525,447, filed Aug. 8, 1995, now abandoned.

BACKGROUND OF THE INVENTION

The present invention relates to a lateral semiconductor arrangement. More specifically, the present invention relates to a lateral semiconductor device used in a power integrated circuit (hereinafter referred to as "power IC") that drives a switching power supply, flat panel display, motor, or other such device.

Referring to FIG. **24**, a cross section of a lateral insulated gate bipolar transistor (hereinafter referred to as an "LIGBT") is shown, as an example of a conventional lateral semiconductor device, integrated into a power IC. This conventional LIGBT includes a p-type substrate **2401** on which an n-type buried layer **2402** is formed. An n-type epitaxial layer **2403** is layered onto n-type buried layer **2402**. An n-type sink layer **2404** extends from a surface of n-type epitaxial layer **2403** to n-type buried layer **2402**. A p-type isolation layer **2405** isolates a device area from the surface of n-type epitaxial layer **2403** to p-type substrate **2401**.

A p-type base region **2407** is in an upper portion of n-type epitaxial layer **2403**. A p-type contact region **2413** and an n-type emitter region **2415** are in p-type base region **2407**. A p-type collector region **2414** is in a surface portion of n-type sink layer **2404**. A thick oxide film **2410** extends over a portion of n-type epitaxial layer **2403** between p-type base region **2407** and n-type sink layer **2404**. A gate electrode **2412**, fixed via a gate oxide film **2411**, extends from n-type emitter region **2415** across a surface of p-type base region **2407** to epitaxial layer **2403**. Gate electrode **2412** is connected to a terminal G. An emitter electrode **2417** contacts both n-type emitter region **2415** and p-type contact region **2413**. Emitter electrode **2417** is connected to a terminal E. A collector electrode **2418** on p-type collector region **2414** is connected to a terminal C. In some devices, an inter-layer insulation film, metal wiring, passivation film, or other such material is formed.

In the above described device, a voltage, higher than a threshold voltage and positive with respect to the potential of emitter electrode **2417**, is applied to gate electrode **2412**. The applied voltage creates an inversion layer in a surface layer of p-type base region **2407** beneath gate electrode **2412**. Electrons flow from n-type emitter region **2415** into n-type epitaxial layer **2403** through the inversion layer where they are injected into collector region **2414**. As a result, the electron current functions as a base current of a pnp transistor consisting of p-type collector region **2414**, n-type epitaxial layer **2403**, and p-type base region **2407**. The base current turns on this pnp transistor to cause conductivity modulation and a large current between the terminals C and E.

However, the device of FIG. **24** has a number of drawbacks. The device of FIG. **24** includes a parasitic pnp transistor Q1 consisting of p-type collector region **2414**, n-type sink layer **2404**, n-type epitaxial layer **2403** and r-type buried layer **2402**, and p-type substrate **2401**. Electrons, as the minority carriers, accumulate in p-type substrate **2401**. Changing state, i.e., switching, requires considerable time to extract and extinguish accumulated electrons, thereby causing a remanent current. The remanent current elongates switching time and increases switching loss.

The device of FIG. **24** also includes a parasitic transistor Q2 consisting of p-type collector region **2414**, n-type sink layer **2404**, and p-type isolation layer **2405**. When the device is used as a high-side switch of a half-bridge circuit or other such circuit, a parasitic current flows from collector electrode **2418** to p-type substrate **2401** through parasitic transistors Q1 and Q2. These parasitic currents increase switching loss.

Referring to FIG. **25**, a cross section of another conventional LIGBT integrated into a power IC is shown. This conventional LIGBT includes a p-type substrate **2501** on which an n-type well region **2503** is formed. A p-type base region **2507** is formed in a part of n-type well region **2503**. An n-type emitter region **2515** and a p-type contact region **2513** are formed in an upper portion of p-type base region **2507**. An emitter electrode **2517** contacts n-type emitter region **2515** and p-type contact region **2513** in common. Emitter electrode **2517** is connected to a terminal E.

An n-type buffer region **2509** is formed in a portion of n-type well region **2503**. A p-type collector region **2514** and an n-type contact region **2516** are formed in an upper portion of n-type buffer region **2509**. A collector electrode **2518** is on p-type collector region **2514**. Collector electrode **2518** is connected to a terminal C. An anode electrode **2519** is on n-type contact region **2516**.

A thick oxide film **2510** on a portion of n-type well region **2503** extends between n-type buffer region **2509** and p-type base region **2507**. A gate electrode **2512** connected to a terminal G is fixed via a gate oxide film **2511** to a portion of n-type base region **2507** extending between a portion of n-type well region **2503** and n-type emitter region **2515**. In devices of this type, an inter-layer insulation film, metal wiring, passivation film, or such material is sometimes formed.

In this conventional device, a voltage, higher than a threshold voltage and positive with respect to a potential of emitter electrode **2517**, is applied to gate electrodes **2512**. The applied voltage creates an inversion layer in a surface layer of p-type base region **2507** beneath gate electrode **2512**. Electrons flow from n-type emitter region **2515** into n-type well region **2503** through the inversion layer, where they are injected into p-type collector region **2514**. As a result, the electron current functions as a base current of a pnp transistor consisting of p-type collector region **2514**, n-type well region **2503**, and p-type base region **2507**. The base current turns on this pnp transistor, causing conductivity modulation and a large current between terminals C and E.

The device of FIG. **25** is less costly than the device shown in FIG. **24** because it does not need any epitaxial wafer such as n-type epitaxial layer **2403**. This device is used as a low-side switch because the device can not be provided with a buried layer. A parasitic transistor Q3 exists consisting of p-type collector region **2514**, n-type well region **2503**, and p-type substrate **2501**. This device is subject to a parasitic current that flows through parasitic pnp transistor Q3 through the same mechanism as described in the above paragraph. Although the prior art is explained by way of an LIGBT, these drawbacks also occur in lateral MOSFET's, bipolar transistors, thyristors, and MOS control thyristors (hereinafter referred to as an "LMCT").

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, an object of present invention is to overcome the drawbacks and limitations of the prior art.